CENG 336
INT. TO EMBEDDED SYSTEMS DEVELOPMENT

Spring 2006
Recitation 04
OUTLINE

• I/O PORTS

• Sample program simulation
I/O PORTS

• PORTA → 6-bit
• PORTB → 8-bit
• PORTC → 8-bit
• PORTD → 8-bit
• PORTE → 3-bit

• How to control data direction?
  → TRIS Registers
• What about peripheral pin sharing?
  → You will configure other related registers

Today, we will talk about only digital I/O properties of the ports.
PORTA

- 6-bit wide
- Data direction register is TRISA(Bank1)

TRISA bit 1 → PORTA pin INPUT
TRISA bit 0 → PORTA pin OUTPUT

Read operation → Read pins
Write operation → Write to the port latch

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CEng336
PORTA

- RA0, RA1, RA2, RA3 and RA5 → Pin sharing with Analog-to-Digital Convertor Module (ADC)

- Configure ADCON1 register (Bank1) for digital I/O

xxxx 011x (0x06) → Makes all PORTA pins digital I/O pin

On a Reset condition, these 5 pins are configured as analog input and read as '0'.
PORTA
RA4/T0CKI

• Pin sharing with TIMER0 for external clock input

• has a Schmitt Trigger Input buffer
What is the Schmitt Trigger buffer?

\[ V_{\text{in}} \quad \rightarrow \quad V_{\text{out}} \]
TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>05h</td>
<td>PORTA</td>
<td>—</td>
<td>—</td>
<td>RA5</td>
<td>RA4</td>
<td>RA3</td>
<td>RA2</td>
<td>RA1</td>
<td>RA0</td>
<td>--0x 0000</td>
<td>--0u 0000</td>
</tr>
<tr>
<td>85h</td>
<td>TRISA</td>
<td>—</td>
<td>—</td>
<td>PORTA Data Direction Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>--11 1111</td>
<td>--11 1111</td>
</tr>
<tr>
<td>9Fh</td>
<td>ADCON1</td>
<td>ADFM</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>PCFG3</td>
<td>PCFG2</td>
<td>PCFG1</td>
<td>PCFG0</td>
<td>--0- 0000</td>
<td>--0- 0000</td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'.
Shaded cells are not used by PORTA.
PORTB

• 8-bit wide
• Data direction register is TRISB (Bank1 & Bank3)

TRISB bit 1 → PORTB pin INPUT
TRISB bit 0 → PORTB pin OUTPUT

Read operation → Read pins
Write operation → Write to the port latch
PORTB

• Each of PORTB pins has an internal pull-up resistor.

• To enable pull-up resistors clear RBPU bit (7th) of OPTION_REG register (Bank1 & Bank3).

• Pull-ups are disabled on reset.
PORTB

### TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>06h, 106h</td>
<td>PORTB</td>
<td>RB7</td>
<td>RB6</td>
<td>RB5</td>
<td>RB4</td>
<td>RB3</td>
<td>RB2</td>
<td>RB1</td>
<td>RB0</td>
<td>xxxx</td>
<td>xxxx</td>
</tr>
<tr>
<td>86h, 186h</td>
<td>TRISB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1111</td>
<td>1111</td>
</tr>
<tr>
<td>81h, 181h</td>
<td>OPTION_REG</td>
<td>RBPU</td>
<td>INTEDG</td>
<td>T0CS</td>
<td>T0SE</td>
<td>PSA</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
<td>1111</td>
<td>1111</td>
</tr>
</tbody>
</table>

Legend: \( x \) = unknown, \( u \) = unchanged. Shaded cells are not used by PORTB.
PORTC

• 8-bit wide
• Data direction register is TRISC (Bank1)

TRISC bit 1 → PORTC pin 1NPUT
TRISC bit 0 → PORTC pin 0UTPUT

Read operation → Read pins
Write operation → Write to the port latch

• PORTC pins have Schmitt Trigger input buffers.
## PORTC

### TABLE 3-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>07h</td>
<td>PORTC</td>
<td>RC7</td>
<td>RC6</td>
<td>RC5</td>
<td>RC4</td>
<td>RC3</td>
<td>RC2</td>
<td>RC1</td>
<td>RC0</td>
<td>xxxx xxxx</td>
<td>ประเทศไทย ประเทศไทย</td>
</tr>
<tr>
<td>87h</td>
<td>TRISC</td>
<td>PORTC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
</tbody>
</table>

Legend: `x` = unknown, `u` = unchanged
PORTD

• 8-bit wide
• Data direction register is TRISD(Bank1)

TRISD bit 1 → PORTD pin INPUT
TRISD bit 0 → PORTD pin OUTPUT

Read operation → Read pins
Write operation → Write to the port latch

• PORTD pins have **Schmitt Trigger** input buffers.
PORTD

• PORTD pins are also Paralel Slave Port (PSP) pins

• PSP mode is disabled by clearing control bit PSPMODE (TRISE<4>).

• PSPMODE bit is cleared on reset.
PORTD

### TABLE 3-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>08h</td>
<td>PORTD</td>
<td>RD7</td>
<td>RD6</td>
<td>RD5</td>
<td>RD4</td>
<td>RD3</td>
<td>RD2</td>
<td>RD1</td>
<td>RD0</td>
<td>xxxxx xxxxx</td>
<td>ㅠㅠㅠ ㅠㅠㅠ</td>
</tr>
<tr>
<td>88h</td>
<td>TRISD</td>
<td>PORTD Data Direction Register</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1111 1111</td>
<td>1111 1111</td>
</tr>
<tr>
<td>89h</td>
<td>TRISE</td>
<td>IBF</td>
<td>OBF</td>
<td>IBOV</td>
<td>PSPMODE</td>
<td>—</td>
<td>PORTE Data Direction Bits</td>
<td>0000  -111</td>
<td>0000  -111</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.
PORTE

• 3-bit wide
• Data direction register is TRISE(Bank1)

TRISE bit 1 $\rightarrow$ PORTE pin 1\text{INPUT}
TRISE bit 0 $\rightarrow$ PORTE pin 0\text{OUTPUT}

Read operation $\rightarrow$ Read pins
Write operation $\rightarrow$ Write to the port latch

• PORTE pins have Schmitt Trigger input buffers.
PORTE

• RE0, RE1 and RE2 → Pin sharing with Analog-to-Digital Convertor Module (ADC)

• Configure ADCON1 register (Bank1) for digital I/O

Look at datasheet page 112 for ADCON1 register.

On a Reset condition, these 3 pins are configured as analog input and read as '0'.
TABLE 3-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on: POR, BOR</th>
<th>Value on all other RESETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>09h</td>
<td>PORTE</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>RE2</td>
<td>RE1</td>
<td>RE0</td>
<td>———— xxx</td>
<td>———— uuu</td>
</tr>
<tr>
<td>89h</td>
<td>TRISE</td>
<td>IBF</td>
<td>OBF</td>
<td>IBOV</td>
<td>PSPMODE</td>
<td>—</td>
<td>PORTE Data Direction Bits</td>
<td>0000 -111</td>
<td>0000 -111</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9Fh</td>
<td>ADCON1</td>
<td>ADFM</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>PCFG3</td>
<td>PCFG2</td>
<td>PCFG1</td>
<td>PCFG0</td>
<td>—0— 0000</td>
<td>—0— 0000</td>
</tr>
</tbody>
</table>

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTE.
Software Tips

; Define variable names (without bothering with; absolute addresses)

CBLOCK 0x20 ;Start of data space.
    Var1: 0 ;0x20
    Var2: 1 ;0x20
    Var16:2 ;0x21
    ACCL: 1 ;0x23
    ACCH: 1 ;0x24
ENDC

; You can always call one thing many names.
ACCA equ ACCL ;alias ACCL
ACCB equ ACCH ;alias ACCH
Software: Pitfalls!

- Bit tests will screw you up! Be careful!
- For example:

```c
movf Register, W
btfsc STATUS, Z
goto NZero
Zero .
    .
Nzero .
```

(WRONG!)
Software: Pitfall!

• Read-Modify-Write instructions: BSF, BCF, ANDWF and XORWF

• RMW instructions can cause SERIOUS PROBLEMS if performed on a port register!

• BCF/BSF PORTn Does the following:
  – Reads in the PORTn byte
  – Clears sets the bit
  – Write the whole byte back.
If the pin is an input:
β The input pin state will be read
β The operation performed on it
β The result sent to the output latch.

β This may not immediately cause problems, but if that pin is made into an output later on, the state of the output latch may have changed from the time it was deliberately set by the code.
Cont’d

If the pin is an output:
¥ The output latch and the actual pin *ought* to be in the same state.
¥ **In practice** sometimes they aren’t.
¥ If you are driving a capacitive load, the pin will take time to respond as it charges and discharges the capacitor. A common problem occurs when using the BSF or BCF directly on a port.

```
BSF PORTB, 0 ; B0 is low before
BSF PORTB, 1
```

B0 may not have time to respond to the first instruction before the second one and second instruction reads B0 as low. **Result B0 never gets set.**
Solution:

Use **shadowed I/O**! (simply a ram location)

- Read the port
- Make your modifications according to previous value of the shadowed I/O and your desire.
- Save the result in the shadowed I/O
- Write back the result to the port
Table lookups

Table
   addwf PCL
   retlw 'A' ;←
   retlw 'B'
   retlw 'C'
   retlw 0x95
   retlw 0xF5

; OR

Table
   addwf PCL
   dt "ABC",0x65,0x75

; Call Table after putting and appropriate value in W
; in this case, W in range of 0-4
QUESTIONS