CENG 336
INT. TO EMBEDDED SYSTEMS DEVELOPMENT

Spring 2006
Recitation 07

OUTLINE

- A/D Module
- Test program simulation for ADC
- LCD Driving Specs

A/D Conversion

- Many sensors used to monitor the real world produce analog or continuous voltage signals.

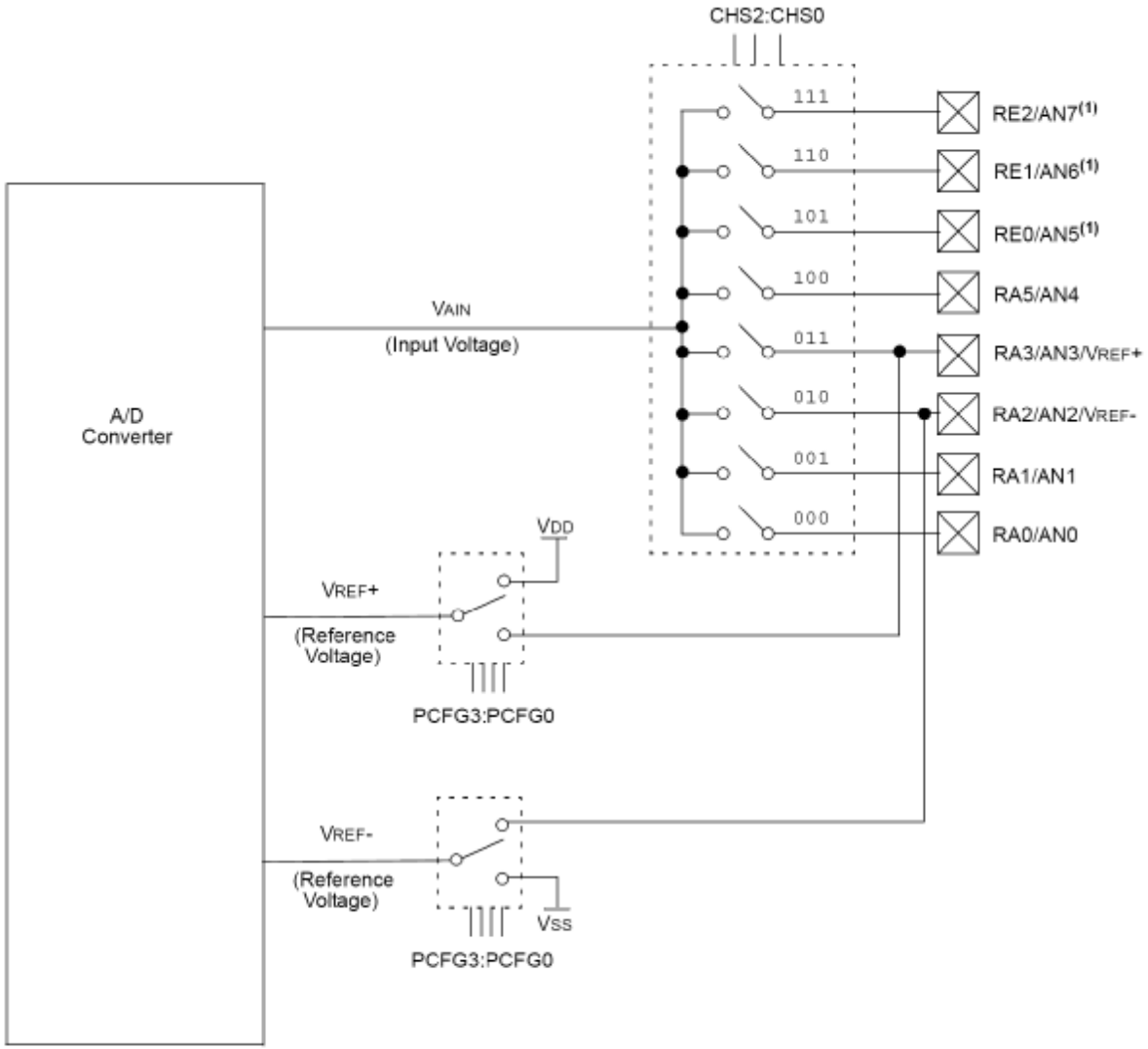
- These signals must be converted to digital form before the computer can process them.

- Analog-to-digital converter (ADC or A/D) converts analog signals to digital signals.

A/D Module in PIC16F877

- 8 Analog input channels
- 10-bit resolution
- Software selectable reference voltages
- Can operate in SLEEP mode using its own internal RC oscillator

Block Diagram



Registers

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register0 (ADCON0)
- A/D Control Register1 (ADCON1)

Registers

REGISTER 11-1: ADCON0 REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = FRC (clock derived from the internal A/D module RC oscillator)

bit 5-3 **CHS2:CHS0**: Analog Channel Select bits
000 = channel 0, (RA0/AN0)
001 = channel 1, (RA1/AN1)
010 = channel 2, (RA2/AN2)
011 = channel 3, (RA3/AN3)
100 = channel 4, (RA5/AN4)
101 = channel 5, (RE0/AN5)(1)
110 = channel 6, (RE1/AN6)(1)
111 = channel 7, (RE2/AN7)(1)

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
If ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1 **Unimplemented**: Read as '0'

bit 0 **ADON**: A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shut-off and consumes no operating current

Registers

REGISTER 11-2: ADCON1 REGISTER (ADDRESS 9Fh)

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified. 6 Most Significant bits of ADRESH are read as '0'.
0 = Left justified. 6 Least Significant bits of ADRESL are read as '0'.

bit 6-4 **Unimplemented:** Read as '0'

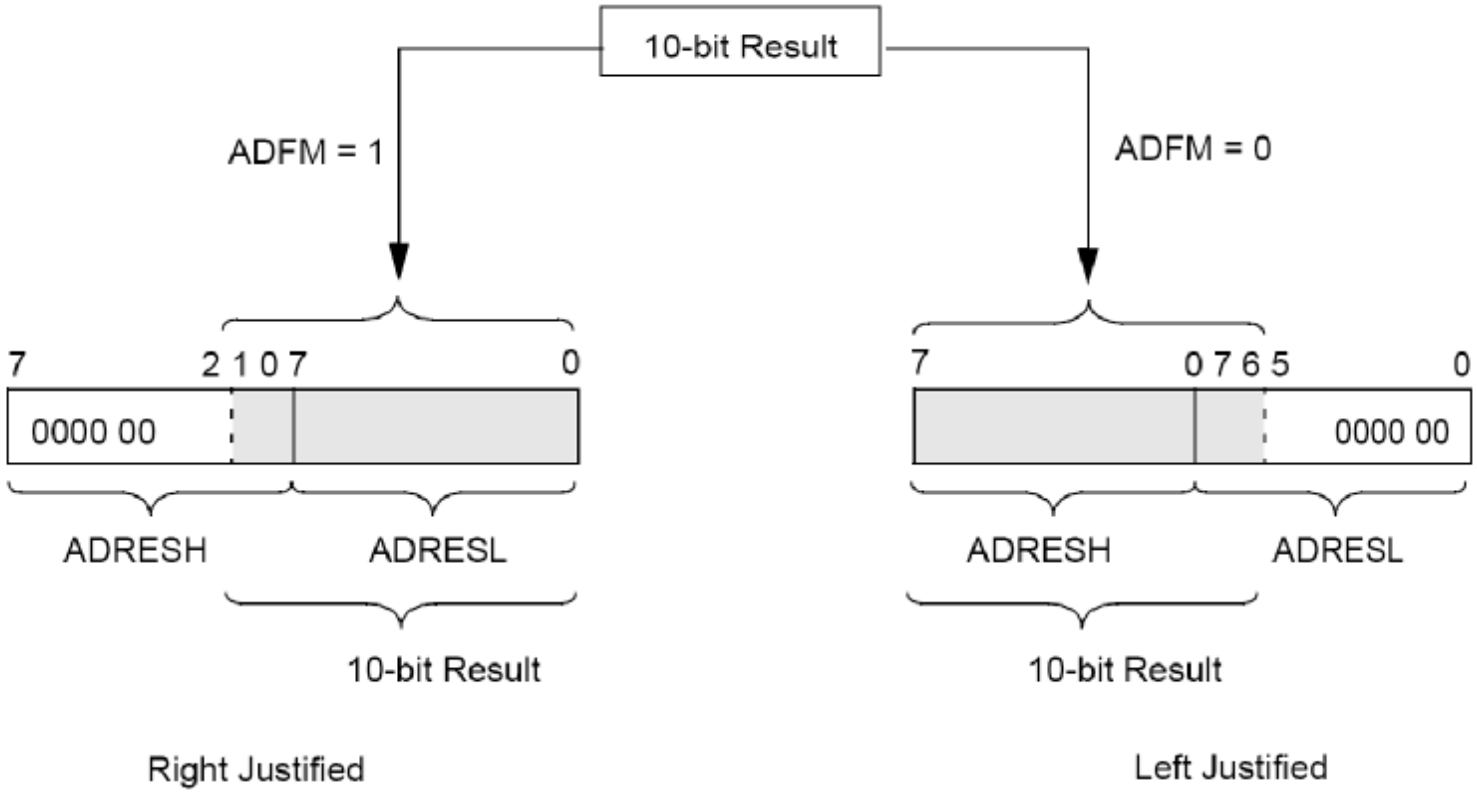
bit 3-0 **PCFG3:PCFG0**: A/D Port Configuration Control bits:

PCFG3: PCFG0	AN7(1) RE2	AN6(1) RE1	AN5(1) RE0	AN4 RA5	AN3 RA3	AN2 RA2	AN1 RA1	AN0 RA0	VREF+	VREF-	CHAN/ Refs(2)
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	RA3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	RA3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	RA3	VSS	2/1
011x	D	D	D	D	D	D	D	D	VDD	VSS	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	RA3	RA2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	RA3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	RA3	RA2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	RA3	RA2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	RA3	RA2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	RA3	RA2	1/2

A = Analog input D = Digital I/O

Registers

A/D Result Justification



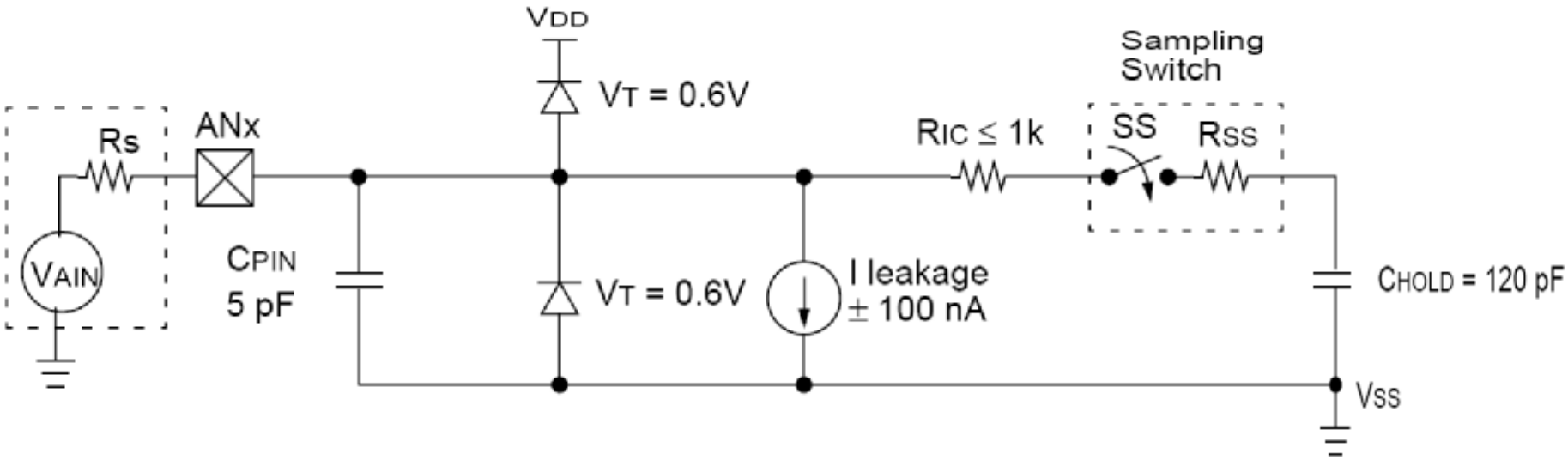
A/D Module Operation

- The analog input charges a sample and hold capacitor.

- The output of the sample and hold capacitor is the input into the converter.

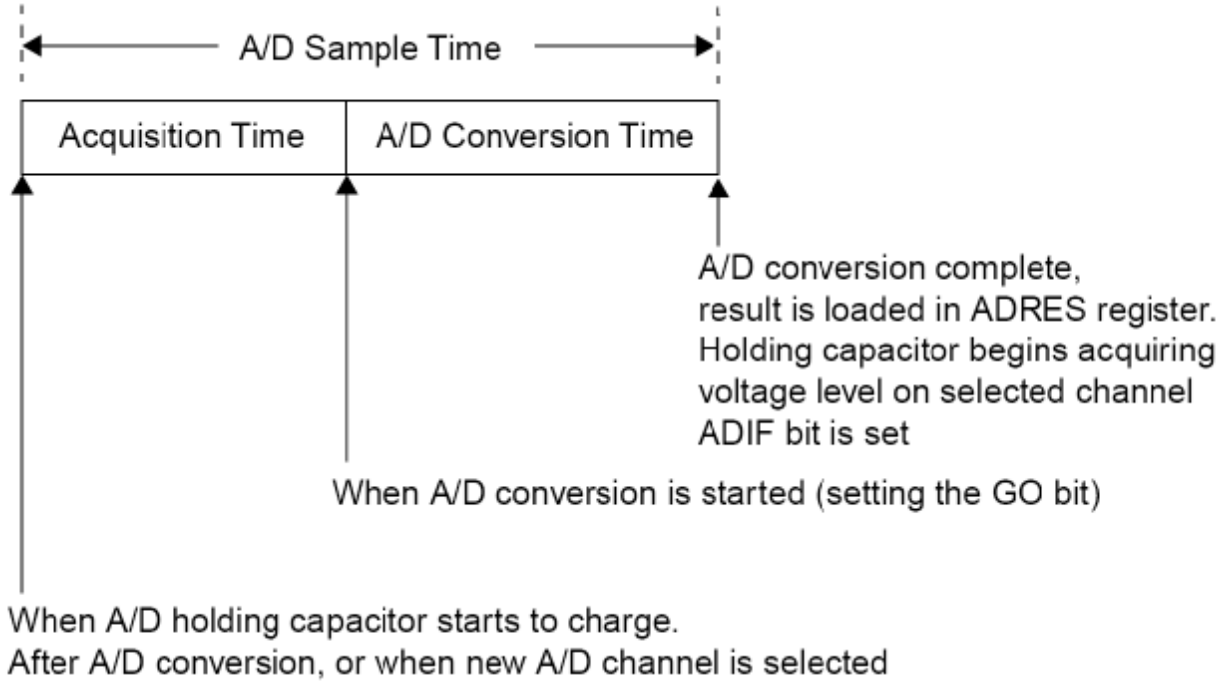
- The converter then generates a digital result of this analog level

Analog Input Model



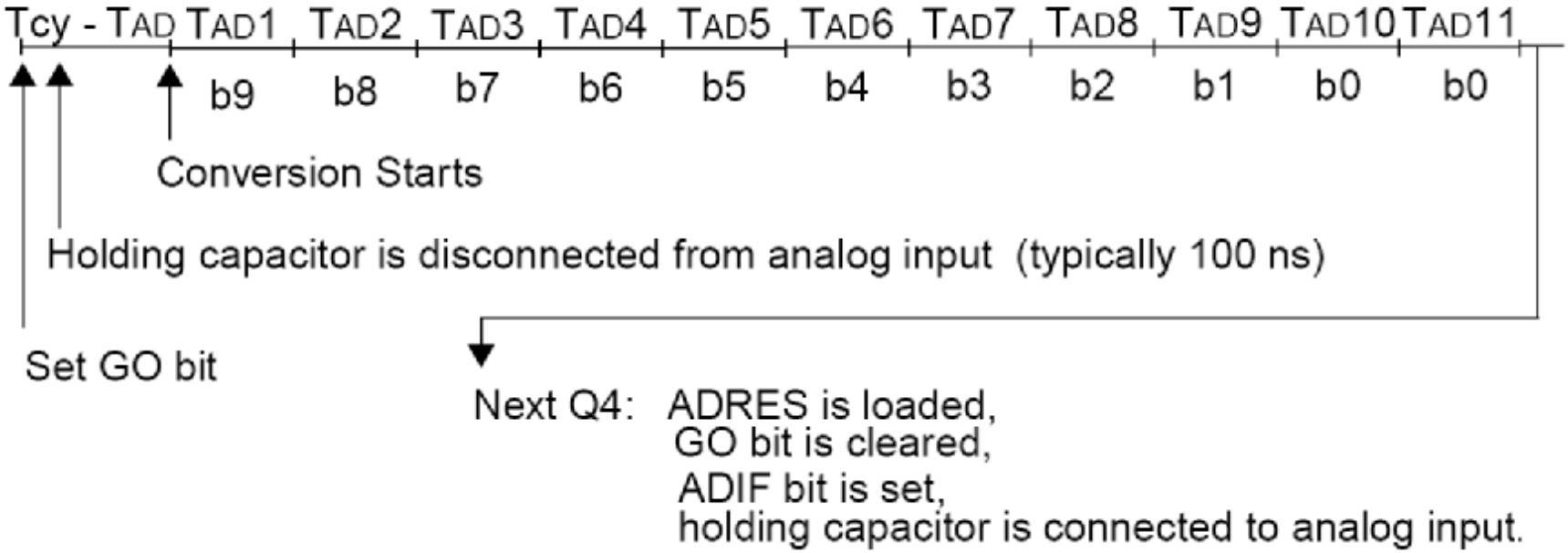
A/D Acquisition Time Requirements

There is a minimum acquisition time to ensure that the holding capacitor is charged to a level that will give the desired accuracy for the A/D conversion. Look at the datasheet for calculations.



A/D Conversion T_{AD} Cycles

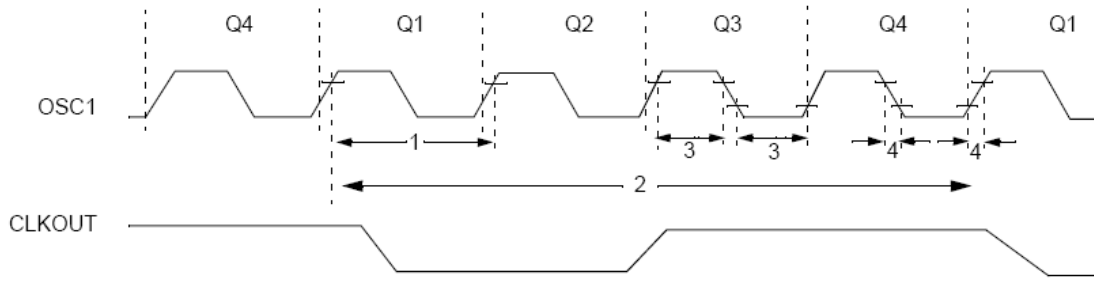
- The A/D conversion time per bit is defined as T_{AD}.
- The A/D conversion requires 11.5-12 T_{AD} per 10-bit conversion.



Selecting A/D Conversion Clock

The four possible options for TAD are:

- 2Tosc
- 8Tosc
- 32Tosc
- Internal RC oscillator



AD Clock Source (TAD)		Device Frequency			
Operation	**ADCS1:ADCS0**	**20 MHz**	**5 MHz**	**1.25 MHz**	**333.33 kHz**
2Tosc	00	100 ns(2)	400 ns(2)	1.6 µs	6 µs
8Tosc	01	400 ns(2)	1.6 µs	6.4 µs	24 µs(3)
32Tosc	10	1.6 µs	6.4 µs	25.6 µs(3)	96 µs(3)
RC	11	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1)

A/D Module Operation

The analog input channels must have their corresponding TRIS bits selected as inputs.

1. Configure the A/D module:
   - Configure analog pins / voltage reference/ and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear the ADIF bit
   - Set the ADIE bit
   - Set the GIE bit
3. Wait the required acquisition time.

A/D Module Operation

4. Start conversion:
   - Set the GO/$\overline{\text{DONE}}$ bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared or ADIF bit to be set

   OR

   - Waiting for the A/D interrupt
6. Read A/D Result register pair (ADRESH:ADRESL), clear the ADIF bit, if required.
7. For the next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as T_{AD}. A minimum wait of $2T_{AD}$ is required before the next acquisition starts.

When the A/D conversion is complete, the result is loaded into this A/D result register pair, the GO/DONE bit (ADCON0<2>) is cleared, and A/D interrupt flag bit, ADIF, is set.

Some Notes

Note 1: When reading the port register, any pin configured as an analog input channel will read as cleared (a low level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

Note 2: Analog levels on any pin that is defined as a digital input (including the AN7:AN0 pins), may cause the input buffer to consume current that is out of the devices specification.

Note: The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D, due to the required acquisition time requirement.

Note 1: On any device reset, the port pins that are multiplexed with analog functions (ANx) are forced to be an analog input.

If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

LCD

LCD Pinouts

Pin	Level	Description	PDB
1	0 V	Ground	GND
2	+5 V	Vcc	+5V
3	Variable	Contrast Voltage	Pot.
4	H/L	"R/S“, H:DATA, L:Instruction	RC0
5	H/L	"R/W“, H:Read (Lcd →Pic), L:Write(Pic → Lcd)	GND
6	H, H→L	"E" Clock input	RC1
7-14	H/L	I/O Pins	PORTD
15	-	Backlight anode	+5V
16	-	Backlight cathode	RA5(INVERTED)

R/S, R/W and E

- The "R/S" bit is used to select whether data or an instruction is being transferred between the microcontroller and the LCD. H:DATA, L:Instruction

- H:Read (Lcd →Pic), L:Write(Pic → Lcd)
On the demo board you can make only write operations since the "R/W" pin is connected to GND.

- After an instruction code or a data presented to the I/O pins a clock pulse should be sent to the "E" pin.

DDRAM Addresses of the Characters

- DDRAM : Display Data RAM
- Relationships between DDRAM addresses (7-bit) and positions on the liquid crystal display.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Display digit
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	DD RAM
Line 3	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	address (HEX)
Line 4	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	

- CGRAM : Character Generator RAM can be used to create custom characters (6-bit address value).
- CGROM : Character Generator ROM generates character patterns.

LCD Instruction Codes

Clear Display

- Clears all display memory and returns the cursor to the home position.

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	1

Return Home

- Returns the cursor to the home position
- DDRAM contents remain unchanged

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	X

Entry Mode Set

• Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	I/D	S

• I/D = 1 : Increment DDRAM address
• I/D = 0 : Decrement DDRAM address

• S = 1 : Display shift [I/D = 1 : Left, I/D = 0 : Right]
• S = 0 : No display shift

Display & Cursor Control

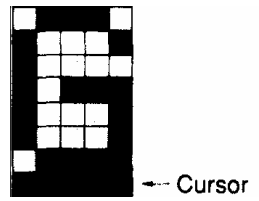
• Sets display (D), cursor (C), and blinking of cursor (B) on/off control bit.

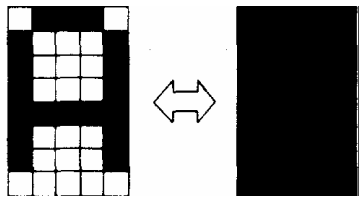
RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	C	B

D = 1 : Display is ON
D = 0 : Display is OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF





Cursor or Display Shift

• Moves the cursor or shifts the display without changing DD RAM contents.

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	S/C	R/L	X	X

S/C	R/L	Operation
0	0	The cursor position is shifted to the left
0	1	The cursor position is shifted to the right
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

Function Set

• Sets interface data length (DL), number of display lines (N), and character font (F).

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	DL	N	F	X	X

DL = 1 : 8-bit
DL = 0 : 4-bit

N = 1 : 2 lines
N = 0 : 1 line

F = 1 : 5x11 dots
F = 0 : 5x8 dots

Set DDRAM Address

- Sets the DDRAM address

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

- Relationships between I/O port values and positions on the liquid crystal display.

Line1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
Line2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF
Line3	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
Line4	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF

Set CGRAM Address

- Sets the CGRAM address

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Write Data to RAM

- Writes data into the RAM

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	D7	D6	D5	D4	D3	D2	D1	D0