CENG 336
INT. TO EMBEDDED SYSTEMS DEVELOPMENT

Spring 2006
Recitation 08

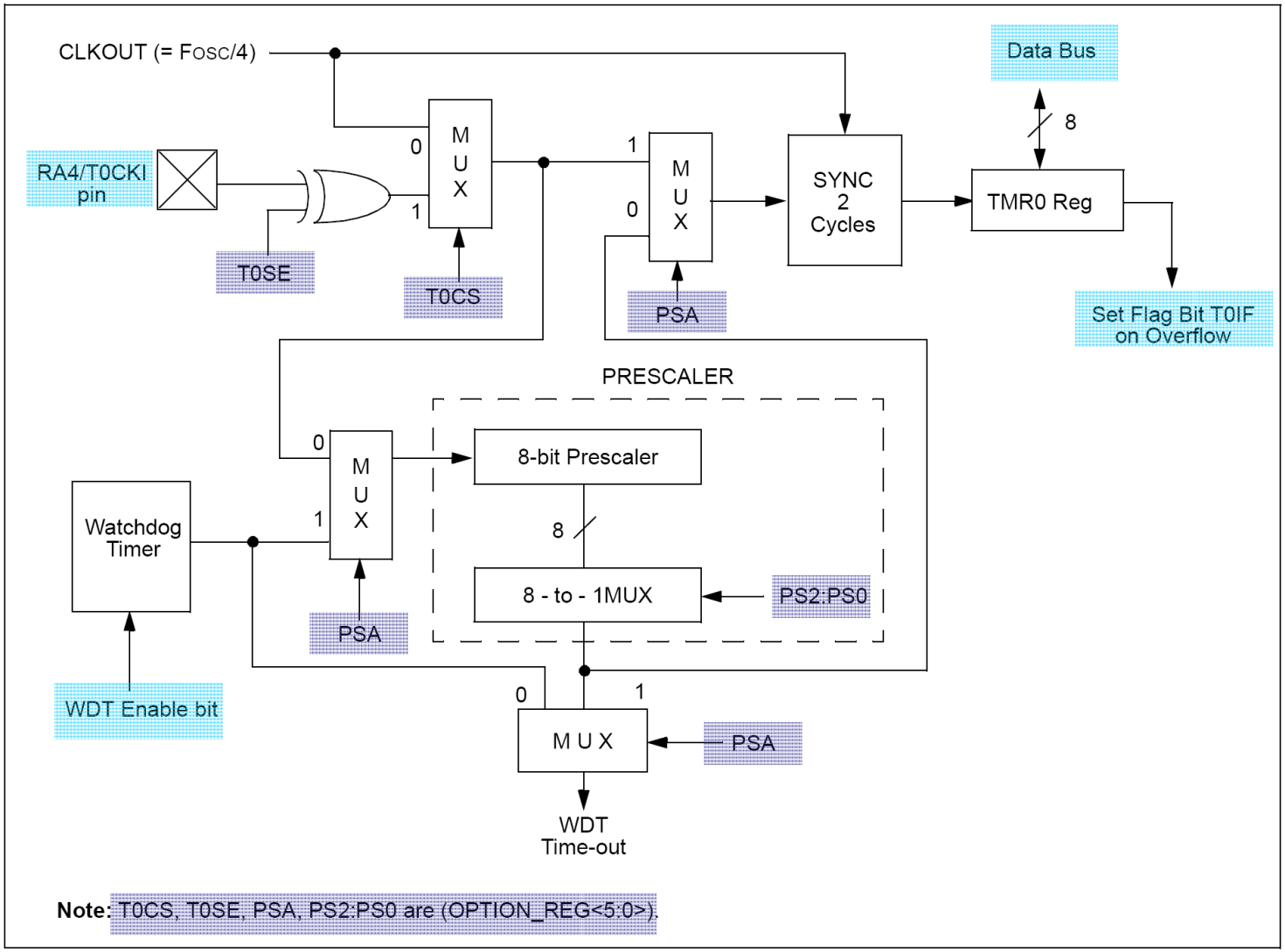
OUTLINE

- TIMER MODULES
  - TIMER0 Module
  - TIMER1 Module
  - TIMER2 Module
- Sample program simulation

TIMER0 Module

- 8-bit timer/counter
- Readable and writable (TMR0 register)
- 8-bit software programmable prescaler
- Internal or external clock select
- Edge select for external clock
- Interrupt on overflow from FFh to 00h

BLOCK DIAGRAM OF THE TIMER0



TIMER MODE

- Timer0 module increments using **internal clock** according to the **prescaler**.
- If the TMR0 register is written, the increment is **inhibited** for the following **two instruction cycles**.
- All instructions writing to TMR0, when the prescaler is assigned to Timer0, will clear the prescaler count, but will not change the prescaler assignment.

OPTION_REG REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

T0CS: TMR0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

PSA: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

PS2:PS0: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

COUNTER MODE

• Timer0 increments either on **rising or falling edge** of pin RA4/T0CKI according to the prescaler.
• All instructions writing to TMR0, when the prescaler is assigned to Timer0, will clear the prescaler count, but will not change the prescaler assignment.

OPTION_REG REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

T0CS: TMR0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

T0SE: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

PSA: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

PS2:PS0: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

TIMER0 INTERRUPT

- TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h.

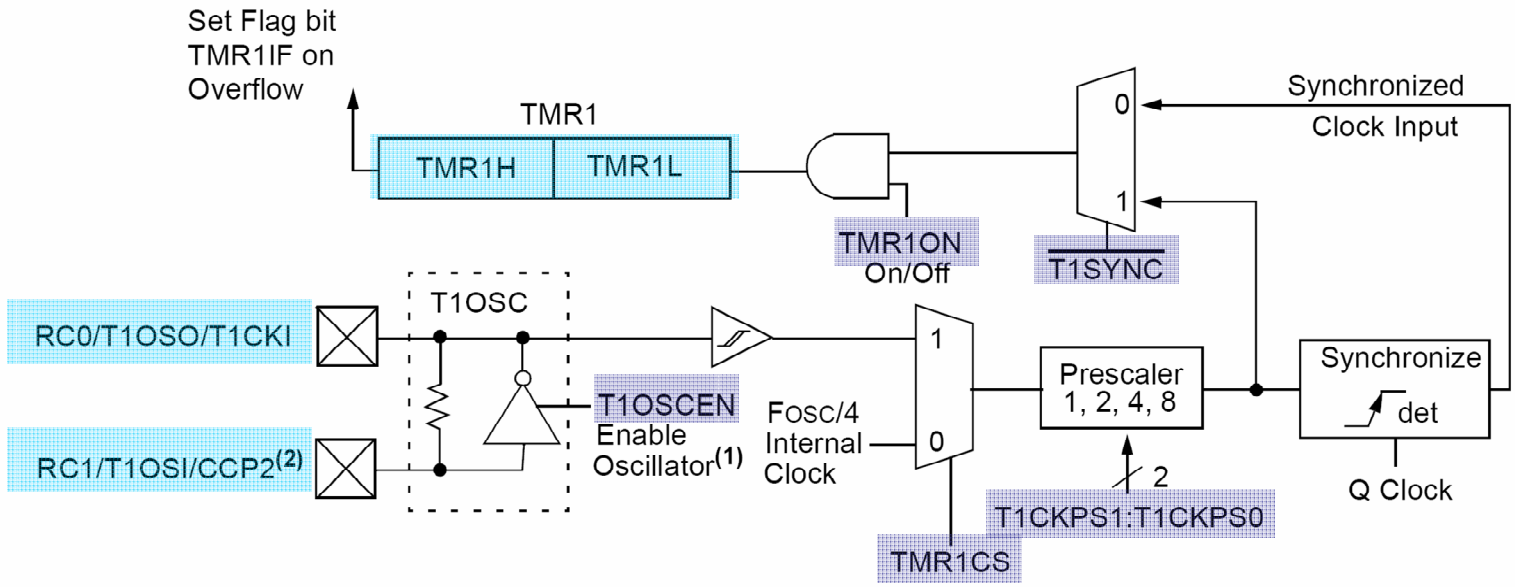
INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit 7							bit 0
		ENABLE BIT			**FLAG BIT**		

TIMER1 Module

- 16-bit timer/counter
- Readable and writable (TMR1H & TMR1L)
- Software programmable prescaler
- Internal or external clock select
- External clock can be syn. or asyn.
- No edge select, only rising edge!
- Interrupt on overflow from FFFFh to 0000h
- Second crystal permitted
- Can be used by CCP modules

BLOCK DIAGRAM OF THE TIMER1



Note 1: When the T1OSCEN bit is cleared, the inverter is turned off. This eliminates power drain.

- When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI/CCP2 and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ignored, and these pins read as ‘0’.
- The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

TIMER MODE

• In this mode, Timer1 module increments using **internal clock** according to the **prescaler**.
• T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset. In any other reset, the register is unaffected.

T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

T1CKPS1:T1CKPS0:
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

TMR1CS: Timer1 Clock Source Select bit
1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)
0 = Internal clock (Fosc/4)

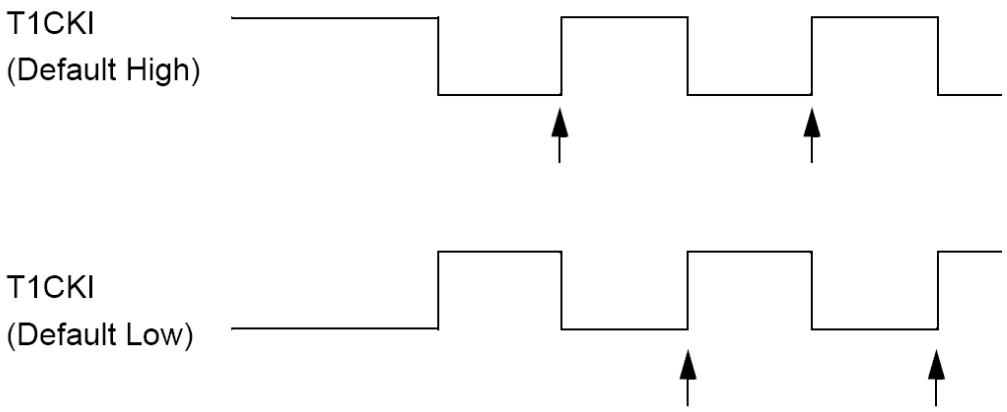
TMR1ON: Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

COUNTER MODE

• In this mode, Timer1 increments either on **rising edge** of the pin

- RC1/T1OSI/CCP2 when T1OSCEN is set
- RC0/T1OSO/T1CKI when T1OSCEN is cleared

• After Timer1 is enabled in Counter mode, the module must first have a falling edge before the counter begins to increment.



COUNTER MODE

T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

T1OSCEN: Timer1 Oscillator Enable Control bit

1 = Oscillator is enabled
0 = Oscillator is shut-off (the oscillator inverter is turned off to eliminate power drain)

$\overline{\text{T1SYNC}}$: Timer1 External Clock Input Synchronization Control bit

When TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input

When TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

TMR1CS: Timer1 Clock Source Select bit

1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)
0 = Internal clock (FOSC/4)

TMR1ON: Timer1 On bit

1 = Enables Timer1
0 = Stops Timer1

TIMER1 INTERRUPT

- TMR1 interrupt is generated on overflow from FFFFh to 0000h

INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit 7							bit 0

PIE1 REGISTER (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

ENABLE BIT

PIR1 REGISTER (ADDRESS 0Ch)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

FLAG BIT

Reading a 16-bit Free-Running Timer

```
; All interrupts are disabled
        MOVF   TMR1H, W    ; Read high byte
        MOVWF  TMPH        ;
        MOVF   TMR1L, W    ; Read low byte
        MOVWF  TMPL        ;
        MOVF   TMR1H, W    ; Read high byte
        SUBWF  TMPH,  W    ; Sub 1st read with 2nd read
        BTFSC  STATUS,Z    ; Is result = 0
        GOTO   CONTINUE    ; Good 16-bit read
;
; TMR1L may have rolled over between the read of the high and low bytes.
; Reading the high and low bytes now will read a good value.
;
        MOVF   TMR1H, W    ; Read high byte
        MOVWF  TMPH        ;
        MOVF   TMR1L, W    ; Read low byte
        MOVWF  TMPL        ;
; Re-enable the Interrupt (if required)
CONTINUE                   ; Continue with your code
```

Writing a 16-bit Free-Running Timer

```
; All interrupts are disabled
        CLRF   TMR1L        ; Clear Low byte, Ensures no
                            ;   rollover into TMR1H
        MOVLW  HI_BYTE      ; Value to load into TMR1H
        MOVWF  TMR1H, F     ; Write High byte
        MOVLW  LO BYTE      ; Value to load into TMR1L
        MOVWF  TMR1L, F     ; Write Low byte
; Re-enable the Interrupt (if required)
CONTINUE                    ; Continue with your code
```

TIMER2 Module

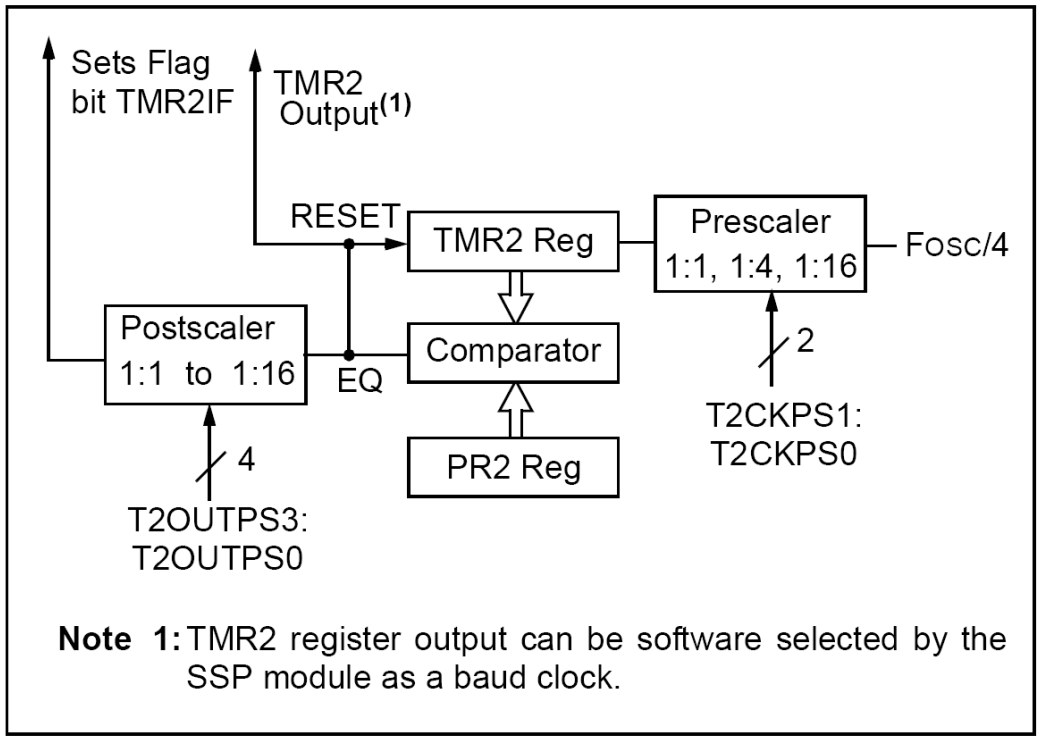
- 8-bit timer only
- Readable and writable (TMR2)
- Cleared on any device reset
- 1:1,1:4 or 1:16 programmable prescaler
- 4-bit programmable postscaler
- Has a period register (PR2)
- Interrupt on match with PR2
- Can be used by CCP modules

BLOCK DIAGRAM OF THE TIMER2

• PR2 is 8-bit readable and writable period register and initialized to FFh upon RESET.

• Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle.

• The match output of TMR2 goes through a 4-bit postscaler to generate a TMR2 interrupt.



• The prescaler and postscaler counters are cleared when any of the following occurs:
  - a write to the TMR2 register
  - a write to the T2CON register
  - any device RESET (POR, MCLR Reset, WDT Reset, or BOR)

TIMER2 CONTROL REGISTER

T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Unimplemented: Read as '0'

TOUTPS3:TOUTPS0: Timer2 Output Postscale Select bits

0000 = 1:1 Postscale
0001 = 1:2 Postscale
0010 = 1:3 Postscale
•
•
•
1111 = 1:16 Postscale

TMR2ON: Timer2 On bit

1 = Timer2 is on
0 = Timer2 is off

T2CKPS1:T2CKPS0: Timer2 Clock Prescale Select bits

00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

TIMER2 INTERRUPT

- TMR2 interrupt is generated on match with PR2 (consider postscaler).

INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit 7							bit 0

PIE1 REGISTER (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

ENABLE BIT

PIR1 REGISTER (ADDRESS 0Ch)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

FLAG BIT

ANY QUESTION?